



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

2814
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In re the Application of: **HASHIMOTO, Hiroshi et al.**

Group Art Unit: **2814**

Serial No.: **09/960,399**

Examiner: **Howard Weiss**

Filed: **September 24, 2001**

P.T.O. Confirmation No.: **5652**

For: **A SEMICONDUCTOR INTEGRATED CIRCUIT AND FABRICATION PROCESS
HAVING COMPENSATED STRUCTURES TO REDUCE MANUFACTURING DEFECTS
(as amended)**

AMENDMENT UNDER 37 CFR §1.111

Commissioner for Patents
Washington, D.C. 20231

Sir:

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Mash
10/8/02
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OCT - 3 2002
TECHNOLOGY CENTER 2800

In response to the Office Action dated **July 2, 2002**, please amend the above-identified application as follows:

IN THE DRAWINGS:

Submitted herewith is a Request for Approval of Drawing Corrections, along with proposed drawing corrections to Figures 1A-30B, as marked in red ink.

The applicants respectfully request that the proposed drawing corrections submitted herewith be approved by the Examiner, and that the outstanding objection to the drawings be withdrawn.